REMARKS

Claims 1 – 8 are pending in this application. Reconsideration in view of the following remarks is respectfully requested. Applicant respectfully submits that this response is fully responsive to the Office Action dated **July 7, 2004**.

Allowable Claim Subject Matter:

Applicant gratefully acknowledges the indication in item 7 of the Office Action that claims 5, 7 and 8 are allowable.

Applicant also gratefully acknowledges the indication in item 6 of the Office Action that claim 4 would be allowable, if amended, to include all of the limitations of the base claim and any intervening claims. However, for at least the reasons stated below, it is respectfully submitted that all of claims 1 – 4 and 6 are allowable.

As To The Merits:

As to the merits of this case, the Examiner relies on the newly cited reference of Ibori et al. (U.S. Patent No. 5,456,202) in setting forth the following rejection:

claims 1 – 3 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Josephson (U.S. Patent No. 4,608,625, of record) in view of Ibori et al.

This rejection is respectfully traversed.

With regard to claim 1, the Examiner acknowledges that "Josephson is silent with regard to including means for short-circuiting the positive and negative terminals upon loss of source power".1

In other words, the Examiner acknowledges that Josephson fails to disclose or fairly suggest the features of claim 1 concerning a short circuit for short-circuiting substantially between said positive polarity voltage outputting terminal and said negative polarity voltage outputting terminal in response to a power-off signal provided by the control circuit.

In order to compensate for the above-noted drawbacks and deficiencies of Josephson, the Examiner relies on the newly cited secondary reference of Ibori.

More specifically, with regard to Ibori, the Examiner asserts:

> As shown in Figure 3, semiconductor switching element 3 short-circuits positive line P and negative line N upon application of a signal from on-off control circuit 12 ("a power-off signal supplied by [a] control circuit"). On-off control circuit 12 receives signal b from input power detecting circuit 13, which detects the off state of the system's power source.2

However, the Examiner is clearly mis-characterizing the teaching of Ibori since switching element 3 is merely a smoothing capacitor whose discharge is controlled by the turning on of semiconductor switching element 11 in response to a control signal "a" or "b" received by

1 Please see, lines 11 – 12, page 3 of the Action.
2 Please see, lines 13 – 16, page 3 of the Action

ON/OFF control circuit 12.

More specifically, according to Ibori:

> When the a.c. power source is interrupted, the signal b is generated after a lapse of the allowable duration time of power stoppage. This signal b is inputted to the ON/OFF control circuit 12 through the OR circuit 14, thereby turning on the semiconductor switching element 11. On the other hand, the signal a is inputted at any time in the same manner as that described with respect to the embodiment shown in FIG. 1, thereby turning on the semiconductor switching element 11.
>
> Since the semiconductor switching element 11 is not turned on at a momentary power stoppage within the allowable duration time thereof, the residual voltage on the smoothing capacitor 3 is not consumed. Thus, a large rush of charging current does not flow into the smoothing capacitor 3 at restarting of the power source, so that the operation of the a.c. machine 4 is continued smoothly. On the other hand, when the momentary power stoppage continues longer than the allowable duration time, the semiconductor switching element 11 is turned on, and the residual voltage of the smoothing capacitor 3 is discharged.3

That is, Ibori is not concerned at all with short circuiting positive line P and negative line N upon application of signal "a" or "b" to on-off control circuit 12. Instead, Ibori discloses that the discharge of smoothing capacitor 3 can be at any time (signal "a") or it can be delayed within the allowable duration time (signal "b") when a.c. power is interrupted in order to avoid a large rush of charging current when the power is restored.

Moreover, the semiconductor switch element 11 of Ibori short-circuits the line P and the line N which are included in a single circuit. In contrast, in the present invention, the output terminals of the first circuit which includes a capacitor and generates the positive polarity voltage

and the second circuit which includes a capacitor and generates the negative polarity voltage are short-circuited.

In view of the above, it is clear that Ibori also fails to disclose or fairly suggest the features of claim 1 concerning a short circuit for short-circuiting substantially between said positive polarity voltage outputting terminal and said negative polarity voltage outputting terminal in response to a power-off signal provided by the control circuit.

In view of the aforementioned remarks, all pending claims are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

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3 Please see, lines 24 – 44, column 4 of Ibori.

In the event that this paper is not timely filed, Applicant respectfully petitionsfor an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

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